



ATK3100A0 PLUTON product brief

PLUTON is a highly optimized 802.11p RFIC, with unique calibration-less architecture to allow uninterrupted operation in harsh vehicular environments.

The PLUTON architecture is based on direct conversion for both the transmitter and receiver, which eliminates expensive and external filters. Support for digitally controlled AGC provides fast gain adaptation, low noise and high dynamic range. The analog baseband filter is calibrated with an internal tuning loop, and the filter supports modulation bandwidths of 10 and 20 MHz. An internal crystal oscillator is implemented to allow the use of a low-cost crystal. A clock output buffer is implemented to deliver a reference frequency for the baseband chip and a potential second PLUTON device. Two fractional-N synthesizers are used to support dual-channel operation. Two frequency bands are supported and the architecture supports 2x2 MIMO operation for the 802.11a,p bands.

An auxiliary Analog-to-digital Converter (ADC) is implemented for calibration purposes and to serve various external functions, such as power and temperature measurements. Control of the chip is done via two four-wire SPI interfaces.

Features

- Transceiver for 802.11p, and 802.11a
- Dual-channel operation with independent synthesizers
- supported frequency band: 5.1-5.925GHz
- Fast channel switching
- High TX linearity – Supports 802.11p mask C with a 6dB margin
- Low noise figure at maximum receive gain.
- Wide RX dynamic range
- Calibration-less RF transceiver
- Two 40MHz SPI slaves
- I2C Slave interface for register access
- Internal Auxiliary ADC

The block diagram below shows the PLUTON transceiver internal blocks:

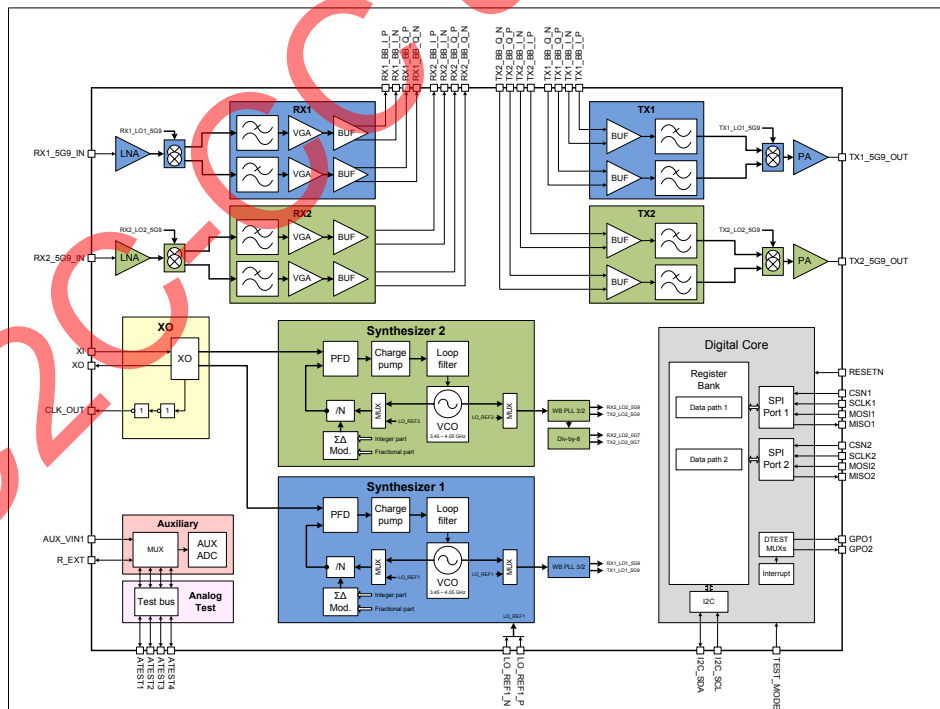


Figure 1: PLUTON Transceiver Block Diagram

1. Device-supported Use Cases

The PLUTON system contains two separate data paths, PHY1 and PHY2, each with its own synthesizer. The two data paths support the frequency band of WAVE in Europe and the US around the 5.9GHz. The two data paths also cover the important 802.11a frequencies (5180÷5825MHz). The data paths and synthesizers can be used concurrently in a number of ways.

A brief summary of major supported use cases is:

- Single Channel, WAVE_EU, WAVE_US
- Dual Channels both channels of IEEE 802.11p
- Diversity, WAVE_EU, WAVE_US
- Dual channels - one channel IEEE 802.11p and one channel IEEE 802.11a
- Channel switching

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2. Device Overview

Receiver Module

The receiver consists of two identical data paths. The main building blocks are the LNA, mixer, passive lowpass filter, active lowpass filter and VGA. The double-sided bandwidth of the analog baseband filter can be adjusted between 10 MHz and 20 MHz with fine resolution around these bandwidths. The receiver gain can be controlled at several positions.

The data path is DC-coupled to avoid settling issues. A DC offset compensation is added before the analog baseband filter in order to mitigate offset errors. The DC offset calibration procedure is performed by the software running in Autotalks Baseband IC.

It is possible to connect the RX baseband signals directly to the Autotalks Baseband IC's ADC inputs.

Transmitter Module

The PLUTON transmitter is built of two identical data paths. The input signal is filtered to suppress Digital-to-analog Converter (DAC) alias signals. A pair of current DACs adds DC currents to minimize the Local Oscillator (LO) leakage. The LO leakage calibration procedure is performed by the software running on Autotalks Baseband IC. The baseband signal is then up-converted and amplified. The RF level at the Power Amplifier (PA) output can be monitored with a peak detector connected to the auxiliary ADC. The peak detector is used to determine appropriate parameters for IQ gain and phase imbalance correction and LO leakage calibration.

Frequency Generation

The two synthesizers are identical. Synthesizer 1 is used in PHY1 and synthesizer 2 is used in PHY2

The reference frequency comes from the crystal oscillator, which is capable of either driving its own crystal or being fed with an external clock. The external clock can be either a sinusoidal signal or a 1.2V CMOS signal. The typical reference frequency is 40 MHz.

Unlock Detector Module

Two sets of unlock detectors are incorporated in PLUTON. One set monitors the synthesizers. The other set continuously monitors the phase of the generated LO signals.

Auxiliary ADC

The PLUTON implements an Auxiliary ADC. The Auxiliary ADC is used during calibration and serves various external functions, such as transmission power and temperature measurements.

Temperature Sensor Module

Temperature information at different chip locations can be measured utilizing the Auxiliary ADC.

SPI Interface

PLUTON is controlled by two independent SPI slave interfaces. Both SPI interfaces have access to the entire register bank, in order to make it possible to control PLUTON with only one SPI. The second SPI port enables having one SPI interface per data path for realtime communication. PLUTON is also equipped with an I²C slave interface for debugging. The I²C interface can also access the entire register bank.

Interrupt Interface

PLUTON supports interrupt signals, one per PHY, each with its own interrupt and mask register.

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3. PLUTON Package

PLUTON is packaged in 9 × 9 mm², 64-pin QFN package.

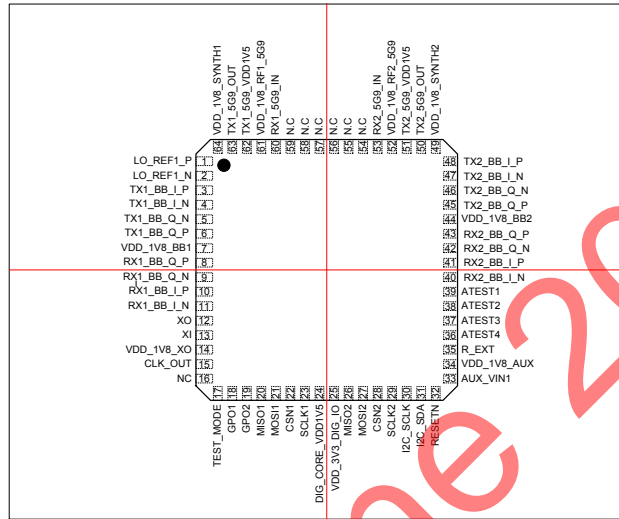


Figure 2: PLUTON Package

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